Listing of Claims:

1. (Previously presented) A phase-change memory device comprising:

a phase-change material layer and a first electrode having a contact area therebetween that extends into a recess of the first electrode to provide current density concentration adjacent thereto, wherein the phase change material layer directly contacts the first electrode throughout the recess.

2. (Original) The phase-change memory device of claim 1, wherein a portion of the phase-change material layer extending into the recess of the first electrode comprises a tapering tip of a vertical part of the phase-change material layer that contacts the first electrode at the contact area.

3. (Original) The phase-change memory device of claim 2, wherein the phase-change material layer further includes a horizontal part extending above the vertical part and wherein the phase-change memory device further comprises a second electrode on the horizontal part.

4. (Original) The phase-change memory device of claim 3, wherein the tapering tip of the vertical part is "V" shaped.

5. (Previously presented) A phase-change memory device comprising:

a phase-change material layer and a first electrode having a contact area therebetween that extends into a recess of the first electrode to provide current density concentration adjacent thereto, wherein a portion of the phase-change material layer extending into the recess of the first electrode comprises a tapering tip of a vertical part of the phase-change material layer that contacts the first electrode at the contact area and wherein the phase-change material layer further includes a horizontal part extending above the vertical part and wherein the phase-change memory device further comprises a second electrode on the horizontal part; and

wherein the first electrode comprises:

a recessed slope part contacting the tip of the vertical part; and

a horizontal part extending from the recessed slope part and separated from the horizontal part of the phase-change material layer by an insulator.

6. (Original) The phase-change memory device of claim 5, further comprising

an integrated circuit substrate;

an interlayer dielectric layer on the integrated circuit substrate;

an insulation layer on the interlayer dielectric layer and having a sloped opening therein; and

wherein the first electrode has a vertical part formed in the sloped opening to provide the recess in the first electrode.

7. (Original) The phase-change memory device of claim 6 further comprising:

a transistor formed in the integrated circuit substrate below the interlayer dielectric layer and having a source region and a drain region; and

a contact plug extending through the interlayer dielectric layer and electrically connecting the first electrode to the source region or the drain region.

8. (Original) The phase-change memory device of claim 7 further comprising an upper dielectric layer on the interlayer dielectric layer and the second electrode and a second electrode contact extending through the upper dielectric layer from the second electrode to contact an upper interconnection.

9. (Original) The phase-change memory device of claim 6, further comprising a sidewall spacer in the sloped opening that separates the vertical part of the first electrode from the insulation layer.

10. (Original) The phase-change memory device of claim 6, wherein the insulation layer includes a first layer on the interlayer dielectric layer and a second layer on the first layer and wherein the sloped opening has a sloped upper portion defined by the second layer and a substantially vertical lower portion defined by the first layer.

11. (Original) The phase-change memory device of claim 10, wherein the first

layer comprises a silicon oxynitride layer and the second layer comprises a silicon oxide layer.

12. (Previously presented) A phase-change memory device comprising:

a phase-change material layer and a first electrode having a contact area therebetween that extends into a recess of the first electrode to provide current density concentration adjacent thereto, wherein a portion of the phase-change material layer extending into the recess of the first electrode comprises a tapering tip of a vertical part of the phase-change material layer that contacts the first electrode at the contact area and wherein the phase-change material layer further includes a horizontal part extending above the vertical part and wherein the phase-change memory device further comprises a second electrode on the horizontal part;

an integrated circuit substrate;

an interlayer dielectric layer on the integrated circuit substrate;

a first insulation layer on the interlayer dielectric layer and having a sloped opening having a first minimum diameter therein, the first electrode having a vertical part formed in the sloped opening and a horizontal part formed on the first insulation layer;

a second insulation layer on the first electrode and having a second opening having a maximum diameter greater than the minimum diameter of the sloped opening therein and extending to the vertical part of the first electrode, wherein the vertical part of the phase-change material layer is formed in the second opening and a horizontal part of the phase-change material layer is formed on the second insulation layer; and

a second electrode on the phase-change material layer.

13. (Original) A phase-change memory device comprising:

a semiconductor substrate;

a first insulation layer on the semiconductor substrate, the first insulation layer having a first opening defined by an upper sloped sidewall part and a bottom vertical sidewall part extending from the upper sloped sidewall part;

a first electrode disposed in the first opening and on the first insulation layer, the first electrode having a recessed slope part in the first opening and a horizontal part on the first insulation layer outside of the first opening;

a second insulation layer on the first electrode, the second insulation layer having a second opening that exposes the recessed slope part of the first electrode;

a phase-change material layer disposed in the second opening and on the second insulation layer; and

a second electrode on the phase-change material layer.

14. (Original) The phase-change memory device of claim 13, wherein the recessed slope part of the first electrode is substantially "V" shaped.

15. (Original) The phase-change memory device of claim 13, wherein:

the first insulation layer includes a stacked silicon oxynitride layer and silicon oxide layer;

the bottom vertical sidewall part of the first opening is defined by the silicon oxynitride layer; and

the upper slope sidewall part of the first opening is defined by the silicon oxide layer.

16. (Original) The phase-change memory device of claim 13, wherein a diameter of the second opening is smaller than a diameter of a bottom opening defined by the bottom vertical sidewall part of the first opening.

17. (Original) The phase-change memory device of claim 15, wherein a diameter of the second opening is smaller than a diameter of the bottom vertical sidewall part of the first opening.

18. (Original) The phase-change memory device of claim 13, wherein the phase-change material layer includes a combination of at least one material selected from the group consisting of Te and Se and another material selected from the group consisting of Pb, Sn, Ag, As, S, Si, P, O and N.

19. (Original) The phase-change memory device of claim 13, wherein:

the first insulation layer comprises a double-layer structure and includes an insulation spacer;

the double-layer structure is formed of a stacked silicon oxynitride layer and silicon oxide layer having an opening therein;

the insulation spacer is arranged on both sidewalls of the opening in the double layer structure;

an upper part of the insulation spacer is sloped and a lower part of the insulation spacer is vertical;

the upper slope sidewall of the first opening is defined by the upper sloped part of the insulation spacer; and

the bottom vertical sidewall of the first opening is defined by the bottom vertical part of the insulation spacer.

20. (Original) The phase-change memory device of claim 19, wherein a diameter of the second opening is smaller than a diameter of the bottom opening defined by the bottom vertical sidewall of the first opening.

21-33. (Canceled).